IN THE CLAIMS:

Rewrite the pending claims as follows:

1-31. (Cancelled).

32. (Previously presented) A memory system, comprising:

a memory module including:

a plurality of memory devices disposed on the memory module;

a supplemental memory device that stores information pertaining to the plurality of memory devices disposed on the memory module; and

an integrated circuit device having controller circuitry that communicates with the plurality memory of devices, the integrated circuit device including:

a receiver circuit to sample receive data from an external signal line at a sample time; and

a first register to store a first value representative of a sampling time adjustment that is applied to the sample time, wherein the first value is determined based on the information pertaining to the plurality of memory devices.

33. (Previously presented) The memory system of claim 32, wherein the sample time is indicated by an internal receive signal, wherein the internal receive signal is adjusted, based on the first value, to apply the sampling time adjustment to the sample time.

34. (Previously presented) The memory system of claim 33, further including a locked loop circuit to generate the internal receive signal.

35. (Previously presented) The memory system of claim 33, wherein the first value is selected such that the sample time is adjusted to substantially center a data eye of the receive data with respect to the internal receive signal.

36. (Previously presented) The memory system of claim 32, wherein the information pertaining to the plurality of memory devices is determined by accessing the supplemental memory device.

37. (Previously presented) The memory system of claim 36, wherein the supplemental memory device is a serial presence detect memory device.

38. (Previously presented) The memory system of claim 32, further including a delay locked loop circuit to generate an internal receive signal, wherein a phase of the internal receive signal is adjusted, based on the first value, to apply the sampling time adjustment to the sample time.

39. (Previously presented) The memory system of claim 32, further including a phase locked loop circuit to generate an internal receive signal, wherein a phase of the internal receive signal is adjusted, based on the first value, to apply the sampling time adjustment to the sample time.

40. (Previously presented) The memory system of claim 32, wherein the sampling time adjustment is a predetermined phase offset that is based on the first value.

41. (Previously presented) The memory system of claim 32, wherein the information pertaining to the plurality of memory devices includes a number of memory devices included in the memory system.

42. (Previously presented) The memory system of claim 32, wherein the integrated circuit device is a dynamic random access memory device.

43. (Previously presented) The memory system of claim 32, wherein the integrated circuit device is a microprocessor device.

44. (Currently amended) The memory system of claim 32, further comprising:

a transmitter circuit to transmit ~~transmit~~ data in response to an internal transmit signal; and

a second register to store a second value representative of a transmit time adjustment that is applied to the internal transmit signal, wherein the second value is determined based on the information pertaining to the plurality of memory devices.

45. (Previously presented) The memory system of claim 44, further including a third register to store a third value representative of a slew rate adjustment that is applied to the transmitter circuit.

46. (Previously presented) The memory system of claim 44, further including a third register to store a third value representative of a drive strength adjustment that is applied to the transmitter circuit.

47. (Previously presented) The memory system of claim 32, further including an additional register to store a value representative of a reference voltage level adjustment that is applied to a reference voltage to derive a modified reference voltage level, wherein the receiver circuit samples the receive data using the modified voltage reference level.

48. (Previously presented) A method of operation in a memory system, wherein the memory system includes an integrated circuit controller device that communicates with a plurality of memory devices, the method comprising:

reading information from a supplemental memory device that pertains to the plurality of memory devices;

determining a first value that represents a sample time adjustment to apply to a sample time of a receiver circuit in the integrated circuit controller device, wherein the sample time adjustment is based on the information from the supplemental memory device; and

storing the first value in a first register on the integrated circuit controller device.

49. (Previously presented) The method of claim 48, wherein the sample time is indicated by an internal receive signal, wherein the method further includes adjusting the internal receive signal based on the first value to apply the sampling time adjustment to the sample time.

50. (Previously presented) The method of claim 49, further including generating the internal receive signal using a locked loop circuit, and wherein adjusting the internal receive signal further includes modifying a circuit element of the locked loop circuit.

51. (Previously presented) The method of claim 49, wherein the first value is selected such that the sample time is adjusted to substantially center a data eye of receive data with respect to the internal receive signal.

52. (Previously presented) The method of claim 49, wherein the sampling time adjustment is applied to the sample time by introducing a phase offset to a phase of the internal receive signal.

53. (Previously presented) The method of claim 48, wherein the supplemental memory device is a serial presence detect memory device.

54. (Previously presented) The method of claim 48, wherein the integrated circuit controller device is a microprocessor device.

55. (Previously presented) The method of claim 48, further comprising:

transmitting transmit data from the integrated circuit controller device to at least one memory device of the plurality of memory devices, in response to an internal transmit signal; and

storing a second value representative of a transmit time adjustment that is applied to the internal transmit signal, wherein the second value is determined based on the information from the supplemental memory device.

56. (Previously presented) The method of claim 55, further including storing a third value that is representative of a slew rate adjustment that is applied to the transmitter circuit.

57. (Previously presented) The method of claim 55, further including storing a third value that is representative of a drive strength adjustment that is applied to the transmitter circuit.

58. (Currently amended) The method of claim 48, further including ~~storing a n~~ storing an additional value representative of a reference voltage level adjustment that is applied to a reference voltage to derive a modified reference voltage level, and sampling in the receiver circuit of the integrated circuit controller device receive data using the modified voltage reference level.

59. (Previously presented) A memory system, comprising:

a memory module including:

a plurality of memory devices disposed on the memory module;

a supplemental memory device that stores information pertaining to the plurality of memory devices; and

a controller device that receives receive data from at least one of the memory devices disposed on the memory module, wherein the controller device includes:

a receiver circuit to sample the receive data in response to an internal receive signal;

a locked loop circuit to generate the internal receive signal based on an external signal; and

a first register to store a first value representative of a sampling time adjustment that is applied to the internal receive signal such that the sample time is adjusted to substantially center a data eye of the receive data with respect to the internal receive signal, wherein the first value is determined based on the information pertaining to the plurality of memory devices.

60. (Previously presented) The memory system of claim 59, wherein the locked loop circuit is a phase locked loop circuit.

61. (Previously presented) The memory system of claim 59, wherein the locked loop circuit is a delay locked loop circuit.

62. (Previously presented) The memory system of claim 59, wherein the external signal propagates along with the receive data.

63. (Previously presented) The memory system of claim 59, wherein the information pertaining to the plurality of memory devices includes module population data.

64. (Previously presented) The memory system of claim 59, wherein the first value is stored in the first register during initialization of the memory module.

65. (Previously presented) The memory system of claim 59, further including a second register to store a second value representative of a reference voltage level adjustment that is applied to a reference voltage to derive a modified reference voltage level, wherein the receiver circuit samples the receive data using the modified voltage reference level.

66. (Currently Amended) The memory system of claim 59, further comprising:

a transmitter circuit to transmit ~~transmit~~ data; and

a second register to store a second value representative of a parameter adjustment that is applied to the transmitter circuit.

67. (Previously presented) A memory system, comprising:

a plurality of dynamic random access memory devices; and

an integrated circuit controller device that communicates with the plurality of dynamic random access memory devices, the integrated circuit controller device including:

a receiver circuit to sample receive data from an external signal line at a sample time that is indicated by an internal receive signal; and

a first register to store a first value representative of a sampling time adjustment that is applied to the sample time by adjusting a phase of the internal receive signal, wherein the first value is determined based on information stored in a serial presence detect memory device.

68. (Previously presented) The memory system of claim 67, further including a locked loop circuit to generate the internal receive signal.

69. (Previously presented) The memory system of claim 67, wherein the first value is selected such that the sample time is adjusted to substantially center a data eye of the receive data with respect to the internal receive signal.

70. (Previously presented) The memory system of claim 67, wherein a serial presence detect memory device is disposed on a memory module substrate along with the plurality of dynamic random access memory devices.

71. (Previously presented) A memory system, comprising:

a plurality of dynamic random access memory devices; and

an integrated circuit controller device that communicates with the plurality of dynamic random access memory devices, the integrated circuit controller device including:

a means for sampling receive data from an external signal line at a sample time that is indicated by an internal receive signal; and

a means for storing a first value representative of a sampling time adjustment that is applied to the sample time by adjusting a phase of the internal receive signal, wherein the first value is determined based on information stored in a serial presence detect memory device.

72. (Previously presented) The memory system of claim 71, further including a locked loop means to generate the internal receive signal.

73. (Previously presented) The memory system of claim 71, wherein the first value is selected such that the sample time is adjusted to substantially center a data eye of the receive data with respect to the internal receive signal.